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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,904	12/18/2001	Andre Zaccarin	42390.P13241	5185

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EXAMINER
SONG, JASMINE

John Patrick Ward
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

ART UNIT	PAPER NUMBER
2188	6

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/024,904	Applicant(s) ZACCARIN ET AL.	
	Examiner Jasmine Song	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment A filed on 02/05/2004, paper # 5. Claims 1-21 are still pending. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The rejection of claims 1-21 under 35 U.S.C. 102(e) as being anticipated by Sherburne are maintained and updated due to the newly amended limitations.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Sherburne JR., US 2002/0169990 A1.

Regarding claims 1, 8 and 15, Sherburne teaches that a method comprising: determining a first memory buffer level (for instance, it is taught as the low water mark of the FIFO 324, col.5, section 0039, last three lines, it indicates FIFO 324 has low water mark level) for at least one memory buffer (the FIFO buffer 324 as shown Fig.2) providing data to digital circuitry (it is taught as the processor 330), determining a second memory buffer level (it is taught as the high water mark of the FIFO 324, see col.3, section 0030) for the at least one memory buffer (the FIFO buffer 324 as shown Fig.2), the second memory buffer level being set greater than the first memory buffer level (the high water mark of the FIFO 324 is set greater than the low water mark of the FIFO 324), comparing data buffer levels in memory (it is taught as BUFFER_FULL, BUFFER_EMPTY) with the first and second memory buffer levels (section 0030 and 0039), and switching digital circuitry from a first state to a second state (it is taught as the controller 322 vary the clock signal to the processor 320 to decrease the processing speed of the processor according to the specification of page 6, 0017, lines 7-9) when the compared data buffer level (it is taught as the BUFFER_FULL) is greater than the second memory buffer level (the high water mark of FIFO 324, col.3, section 0030), and switching the digital circuitry from a second state to a first state (it is taught as the controller 322 vary the clock signal to the processor 320 to increase the processing speed of the processor) when the compared data buffer level (it is taught as the

BUFFER_EMPTY) is less than the first memory buffer level (the low water mark of FIFO 324, col.4, section 0035 and col.5, section 0039).

Regarding claims 2, 9 and 16, Sherburne teaches further comprising switching the digital circuitry between additional states (it is taught as varying the clock frequency to the processor) in response to changing levels of memory buffer data in the at least one memory buffer (it is taught as in response to changing the FIFO in between FULL and EMPTY, col.2, section 0022).

Regarding claims 3, 10 and 17, Sherburne teaches the first and second memory buffer level are augmented by at least one additional memory buffer level (FIFO_FULL or FIFO_EMPTY or in between) to permit greater switching control of the digital circuitry between states in response to compared data buffer levels (col.4, section 003 and col.5, section 0039).

Regarding claims 4, 11 and 18, Sherburne teaches switching the digital circuitry from the first state to the second state further comprises adjusting clock frequency of the digital circuitry (col.2, section 0021, last four lines).

Regarding claims 5, 12 and 19, Sherburne teaches switching the digital circuitry from the first state to the second state further comprises adjusting voltage of the digital circuitry (col.2, section 0021, last four lines).

Regarding claims 6, 13 and 20, Sherburne teaches the digital circuitry is a processor (for instance, col.2 section 0022) directly controlled to switch between states (the processor as shown in Fig.1 and 2).

Regarding claims 7, 14 and 21, Sherburne teaches the digital circuitry is a processor controlled to switch between states in response to interactions with a power management controller (col.2, section 0015 and section 0021).

Response to Arguments

6. Applicant's arguments filed on 02/05/2004 regarding independent claims have been fully considered but they are not persuasive.

7. In response to the applicant's argument that Sherburne does not appear to teach or suggest determining a first memory buffer level, determining a second memory buffer level, and comparing data buffer levels in memory with the first and second memory buffer levels (see applicant's remark's page 12, last paragraph and page 13,first paragraph), however, the Examiner notices that the determining steps is taught as defining the high water mark in section 0030, lines 3, in addition, Sherburne teaches establishing the low-water marks (section 0037, lines 4-5). Sherburne also teaches comparing data buffer levels in memory with the first and second memory buffer levels (in this case, data buffer levels such as BUFFER_FULL or BUFFER_EMPTY compares with the high water mark and low water mark respectively, sections 0030, 0035 and

0039, please refer back to the rejection as shown above). Therefore, Sherburne teaches the claimed invention. In addition, applicant must discuss the references applied against the claims, explaining **how** the claims avoid the references or distinguish from them, however, the arguments filed on 02/05/2004 has only generic statement regarding the reference without specifically addressing the points set-forth in the Examiner's rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30 (first Friday off).
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

JACK A. LANE
PRIMARY EXAMINER

Jasmine Song
Patent Examiner
April 15, 2004

Mano Padmanabhan
Supervisory Patent Examiner
Technology Center 2100